Technical Data

Vector Output I/O Module 9100A-017

```
GROUPS   [16-1] [24-17] [25] [26] [27] [40-28]
DISPLAY      HEX, HEX, BIN, BIN, BIN

! TIME   DATA
!        ADDR                DATA      R/W-  CE-  RESET      UNUSED

! initialize the UUT
   1     $FFFF               $XX       1     1    0          XXXXXXXXXXXXX
   2     $FFFF               $XX       1     1    1          XXXXXXXXXXXXX
   3     $FFFF               $XX       1     1    0          XXXXXXXXXXXXX
! write ten times
loop 10
   4     $0000               $XX       1     1    0          XXXXXXXXXXXXX
   5     $0000               $XX       1     1    0          XXXXXXXXXXXXX
   6     $0000               $XX       1     1    0          XXXXXXXXXXXXX
! wait for UUT handshake
wait +
   7     $0000               $01       0     0    0          XXXXXXXXXXXXX
   8     $0000               $01       0     0    0          XXXXXXXXXXXXX
   9     $0000               $01       1     0    0          XXXXXXXXXXXXX
endloop
   10    $0000               $XX       1     1    0          XXXXXXXXXXXXX
```

Figure 1. Typical Vector File Definition.

The Fluke 9100A-017 Vector Output I/O Module adds high speed test capabilities to the 9100A Digital Test System and 9105A Digital Test Station. The 9100A-017 generates vectors (parallel patterns) using clock speeds up to 25 MHz for functional testing and troubleshooting. High speed parallel stimulus and bus emulation for both microprocessor and non-microprocessor based boards are accomplished using the 9100 Series with the Vector Output I/O Module.

High Speed Parallel Stimulus

The parallel digital vectors may be up to 8192 bits deep. With 40 pins per module, four modules can be used together for a total of 160 pins. Because a loop set of vectors can be defined, this set of vectors can be repetitively output from 1 to 65,536 times. Vectors can be clocked out at up to 25 MHz using an external clock source. Each 40 pin module also provides an internal clock generator for 1, 5, 10, and 20 MHz. The clocks can be qualified by the external lines start, stop and enable.The vectors can also be synchronized to each microprocessor read or write cycle. Each ouput pin can be separately tri-stated for any clock period, or an external tri-state input can simultaneously control all 40 pins on each module.

Response Measurement

The input specifications are identical to those of the 9100A-003 Parallel I/O Module. Responses may be gathered at clock speeds up to 10 MHz for signature analysis and frequency/count measurement. The 9100 Series' single point probe can be used in conjunction with the 9100A-017, acquiring signature, frequency, count, and logic levels at clock speeds up to 40 MHz.

Bus Emulation

The Fluke 9100 Series and the 9100A-017 Vector Output I/O Module, with high speed vector generation, can emulate many common busses. An external input, WAIT, synchronizes the output vectors to the bus cycle ready state. Separate drive and receive clocks allow the vectors to be driven independently of the data input sampling.

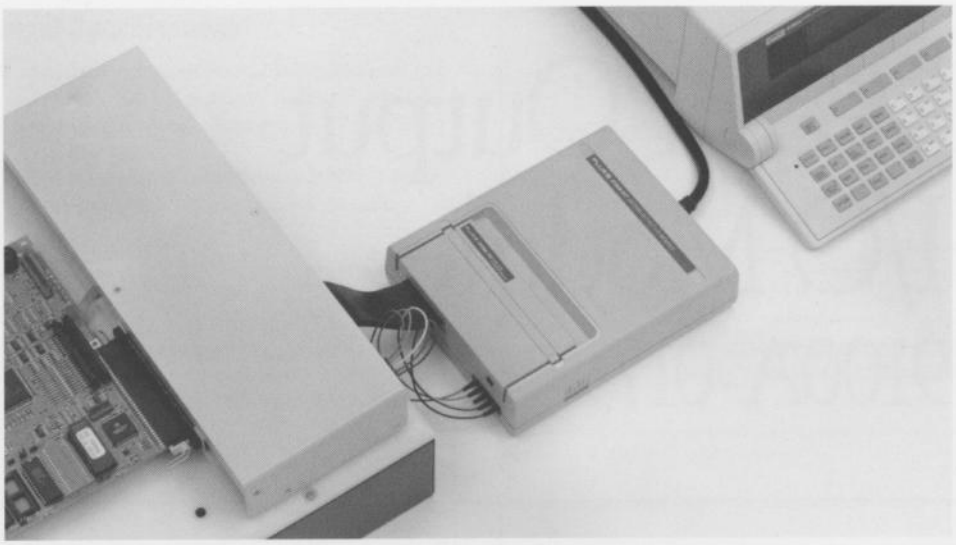
Test Vector Pattern Generation

The generation of test vector patterns can be accomplished in two ways. The 9100A Editor can enter test vectors, or test vectors generated on another computer can be downloaded as text files into the 9100A. Once they are in the 9100A, these files can be modified and translated into 9100A vectors suitable for use with the 9100A-017.

Vectors can be entered in user-defined groups in either hexadecimal or binary notation. The vector editor visually displays the vector information ordered by the pin assignment and arranged in time.

Test Language (TL/1) functions have been added to make use of the new capabilities of the 9100A-017. Loading the vectors from the 9100A hard disk to each module during program execution requires a maximum of 3 seconds, with 1 second typical.

FLUKE



Vector Output I/O Module Connected to a Card Edge Fixture and the 9100A.

The 9100A-017 Vector Output I/O Module is an extension to the test capabilities of the 9100 Series digital testers. It provides the ability to stimulate a circuit card at high data rates, usually at the card edge. Response measurements can then be made with the 9100A's or 9105A's usual test methods to determine the functionality of the board and to isolate any faults. Figure 2 shows the architecture of the 9100A-017, its input and output sections, and the signals that are available to control the vector output and the response measurements.

Definitions

Drive Clocks

There are four signal sources which can clock each step of the vector output. These are:

1. External Drive Clock (DR CLK)

An external clocking signal, selected by the user, and supplied by the UUT (Unit Under Test).

2. Internal Drive Clock (INT CLOCK)

A clocking signal supplied by an oscillator internal to the 9100A-017 Module. The user can select any one of four clocking frequencies.

3. Pod Sync Clock

A clocking signal supplied by the 9100A or 9105A, which is synchronized to a microprocessor bus control line such as "data valid" or "address valid". The actual signals available will depend on the interface pod type.

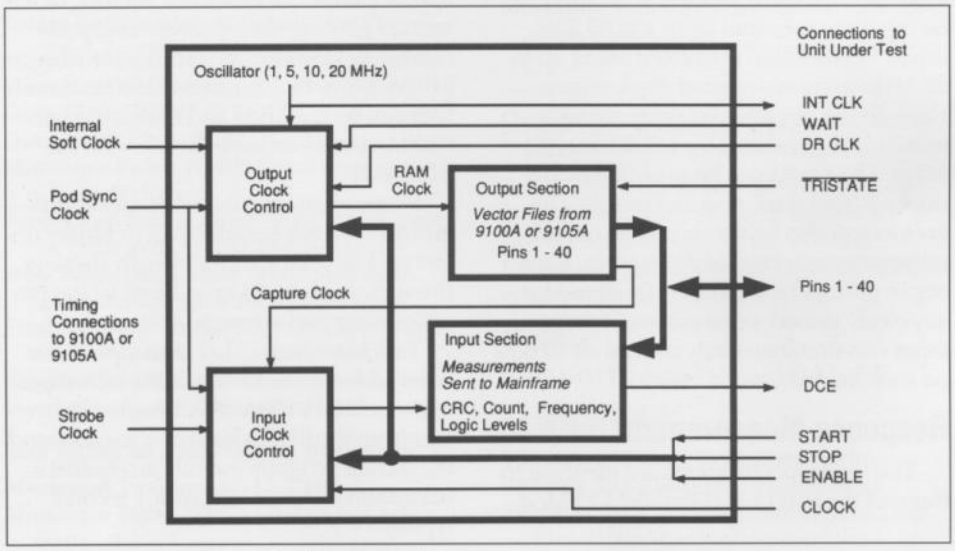


Figure 2. 9100A-017 Control and Timing Architecture

4. Internal Soft Clock

A clocking signal executed on demand from a TL/1 program, as defined by the user. This clock is software generated and can be used to "single step" the vector output in debugging a user program.

Handshake Line (WAIT)

A WAIT command in a vector file stops the vectors from being output until the WAIT line signal edge is received. WAIT commands are programmed into the vector file as shown in Figure 1, and can specify either positive or negative going edges. The WAIT input is connected to a UUT or a bus, to provide "handshake" timing between the 9100A-017 and the UUT. This is useful for synchronizing vectors to events such as "DTACK" or "BUSY". The vector output pins are latched to their last state when a WAIT command is executed.

External Tri-state (TRISTATE)

A single input line that causes all the output pins to be tri-stated. This can be used to initialize the vector output, for example prior to a WAIT signal. It is useful when the 9100A-017 simulates a peripheral on a bus.

Clock Qualifiers (START, STOP, ENABLE)

Control lines which define the valid time window for strobing valid data in or clocking vectors out.

Input Clock (CLOCK)

The input section of the 9100A-017 has its own externally sourced clock input, so that input measurements may be clocked independently of the output section.

Capture Clock

A clock signal programmed as a command line in a vector file, which strobes the input section of the 9100A-017. It provides internal synchronization between the vector outputs and input measurements.

Strobe Clock

A TL/1 programmed clock signal for strobing the input section of the 9100A-017, independent of the output section.

Data Compare Equal (DCE)

A signal that becomes active upon asynchronous detection of a user programmed pattern at the input.

Technical Specifications

Output Specifications

Output specifications were determined using a Fluke Y9100A-102 Card Edge Interface Module connected to 10 LS loads. Actual output results will vary depending on the impedance, length, and shielding of the connections used.

Vector Width (with one module): 40 channels.

Vector Width (with the maximum four modules): 160 channels.

Vector Depth (without looping): 8,192 vectors.

Vector Looping: Up to 65,536 repetitions of any one vector loop set. Multiple loop sets are allowed within a vector file. Each loop set must contain a minimum of two vectors.

Output Logic Levels

High: 3.7V minimum (6.0 mA source).
Low: 0.4V maximum (6.0 mA sink).

Drive Clock Sources:

External Drive Clock (DR CLK): 25 MHz Maximum (maximum may be exceeded in some cases, depending on the impedance, length, and shielding of the connection to the unit under test (UUT)). Minimum pulse width 4.5 ns high or low.

Internal Drive Clock (INT CLK): 1, 5, 10, or 20 MHz, ±100 ppm.

Pod Sync Clock: Available drive clock pod sync modes will depend on the interface pod type.

Internal Soft Clock: Executed from a TL/1 program.

Vector Out Time Delay From Clock Source. *See Figure 3:* Delay (t_{del}) from DR CLK to vector out 50 ±8 ns. Delay (t_{del}) from INT CLK to vector out 37.5 ±7.5 ns.

Handshake Line (WAIT) Setup Time (t_{wsu}). *See Figure 4:* 42.5 ns maximum (35 ns typical) from WAIT edge until a clock cycle drives vector out. If the setup time is not met, the next clock will drive out the vector.

Single Module Channel to Channel Skew: 6 ns maximum (1 ns typical).

Multiple Module Channel to Channel Skew: 10 ns maximum (1 ns typical).

External Tri-state

See Figure 5:

Tri-state Activation Setup Time (t_{xout}): Output drive released 20 ±5 ns after $\overline{\text{TRISTATE}}$ goes low. Minimum $\overline{\text{TRISTATE}}$ pulse width 10 ns.

Tri-state Recovery Setup Time (t_{xsu}): $\overline{\text{TRISTATE}}$ must go high within 5 ns after the rising edge of INT CLK, or within 10 ns after the selected edge of DR CLK. If the setup time is not met, the next vector is skipped over while the output remains tri-stated; the following clock will output the next vector.

Capture Clock Delay (t_{cap}): *See Figure 6:* Delay from non-clocking edge of DR CLK 55 ±10 ns. Delay from falling edge of INT CLK 42.5 ±5 ns.

Start, Stop, and Enable Setup Times:

See Figure 7:

Start Setup Time (t_{str}): 20 ns before DR CLK, 30 ns before INT CLK maximum.

Stop Setup Time (t_{stp}): 20 ns before DR CLK, 30 ns before INT CLK maximum.

Enable Setup Time (t_{en}): 15 ns before DR CLK, 25 ns before INT CLK maximum.

Enable Hold Time (t_{enhld}): 35 ns after DR CLK, 20 ns after INT CLK

Control Line Input Impedance

External Drive Clock (DR CLK): 40 kΩ minimum, 35 pF maximum.

External Tri-state ($\overline{\text{TRISTATE}}$): 40 kΩ minimum, 80 pF maximum.

Handshake (WAIT): 40 kΩ minimum, 50pF maximum.

Vector Output Series Termination: 33 Ω.

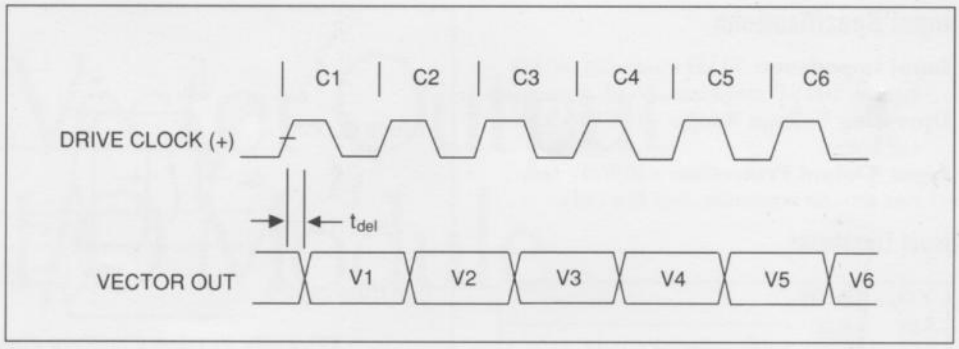


Figure 3. Vector Out Delay from Clock Source

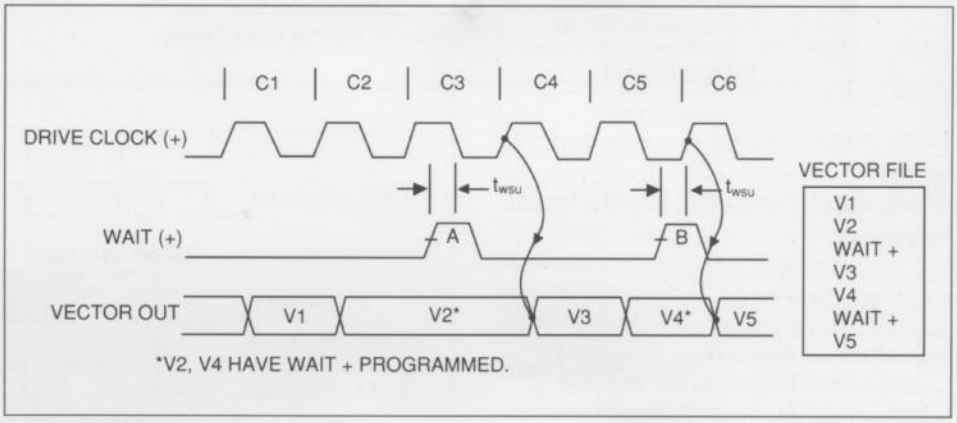


Figure 4. WAIT Input Timing Diagram

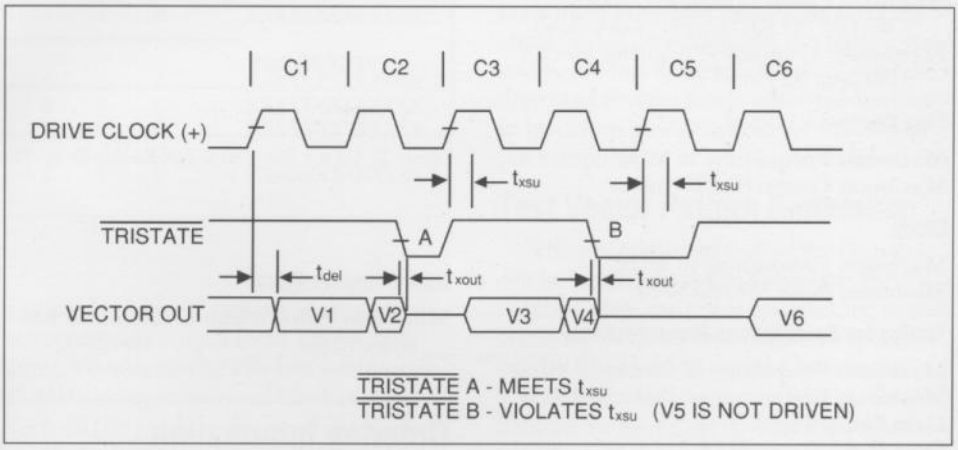


Figure 5. $\overline{\text{TRISTATE}}$ Input Timing Diagram

Input Specifications

Input Impedance: 50 kΩ minimum. 90 kΩ typical. 100 pF maximum. 65 pF typical.
Operating Voltage Range: -0.5V to +5.5V (all lines).
Input /Output Protection: +10V/-5V for one minute maximum, one line only.

Input Thresholds

TTL	CMOS	
5.0V	5.0V	
		Guaranteed HIGH
2.6V	3.4V	
		HIGH or INVALID
2.1V	2.9V	
		Guaranteed INVALID
1.0V	1.2V	
		LOW or INVALID
0.6V	0.8V	
		Guaranteed LOW
0.0V	0.0V	

Clock, Start, Stop, and Enable Inputs

Thresholds

Logic LOW: 0.8V maximum.
Logic HIGH: 2.0V minimum.
Input Current: +1 µA, -125 µA.
Input/Output Protection: +10V/-5V for one minute maximum, one line only.

Transition Counter

Maximum Frequency: 10 MHz.
Maximum Count (Transition Mode): 8,388,608 (23 bits) counts (+ overflow).
Frequency Accuracy (Frequency Mode): ±250 ppm ±2 Hz.

Stop Counter

Maximum Frequency: 10 MHz.
Maximum Count: 65,535 clocks.

Clock

Maximum Frequency: 10 MHz.
Minimum Pulse Width: 50 ns.

Timing for Synchronous Measurements

Maximum Frequency of Clock: 10 MHz.
Maximum Frequency of Data: 5 MHz.
Data Setup Time: 30 ns.
Data Hold Time: 30 ns.
Minimum Pulse Width (Start/Stop/Enable/Clock): 50 ns.
Start Edge Setup Time (before clock edge, for clock to be recognized): 0 ns.
Stop Edge Hold Time (after clock edge, for clock edge to be recognized): 5 ns.
Enable Setup Time (before clock edge, for clock edge to be recognized): 0 ns.
Enable Hold Time (after clock edge, for clock edge to be recognized): 10 ns.

Data Timing for Asynchronous Measurements

Maximum Frequency: 10 MHz.
Minimum Pulse Width (HIGH or LOW): 50 ns.
Minimum Pulse Width (tri-state): 150 ns.

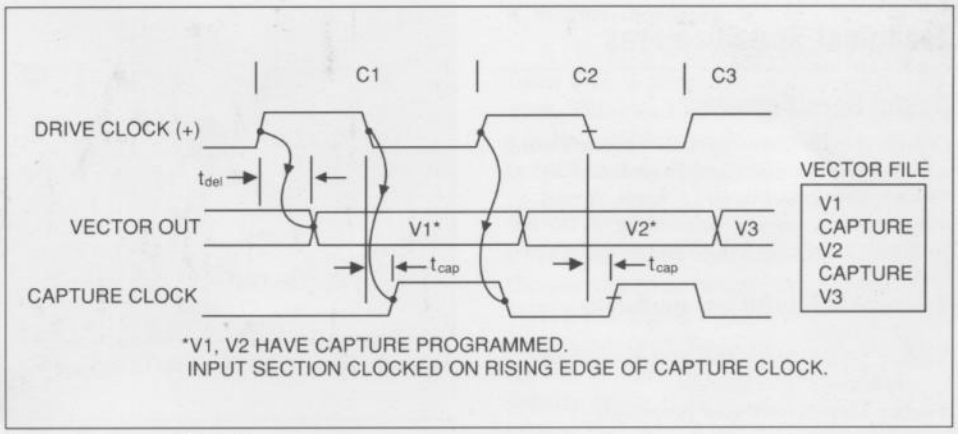


Figure 6. Capture Clock Timing

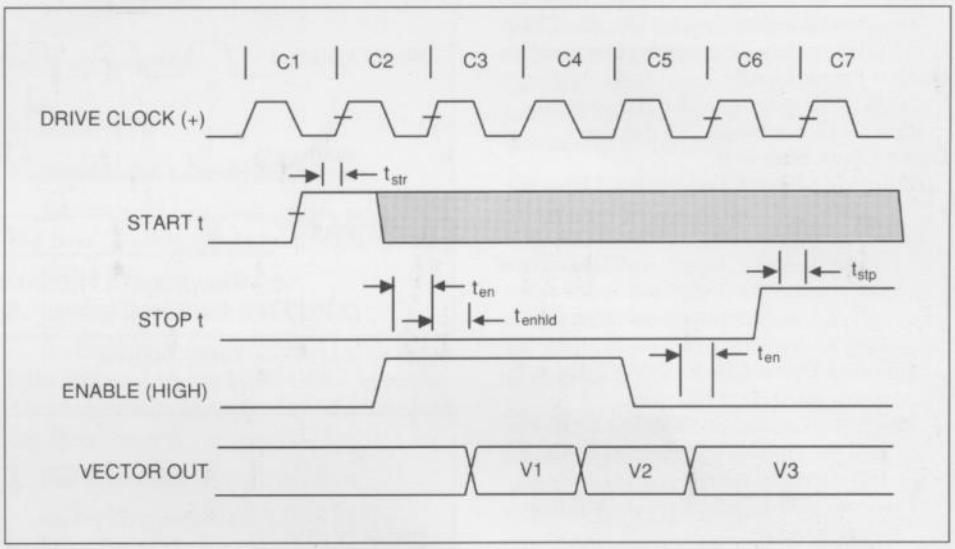


Figure 7. Vector Start, Stop and Enable Setup Times

Data Compare Equal

Minimum Pulse Width of Data and Enable: 75 ns.

Ordering Information

Your 9100A Digital Test System or 9105A Digital Test Station requires Version 4.1 or later software to support the 9100A-017. Four megabytes of internal RAM memory is recommended.

Model

9100A-017 Vector Output I/O Module

Accessories

Y9100A-100 Card Edge Fixture Kit
Y9100A-101 Card Edge Fixture Base
Y9100A-102 Card Edge Interface Module Plus 9100A standard clip modules

John Fluke Mfg. Co., Inc.
P.O. Box C9090, Everett, WA 98206
Tel. (206) 347-6100

For more information call:
(800) 443-5853 (toll-free) in the U.S.A.
(416) 890-7600 in Canada.
(206) 356-5500 from other countries.

Philips International B.V.
T&M Dept., Building TQIII-4
5600 MD Eindhoven, The Netherlands
Telex: 35000 PHTC NL/NLFEVSI

Printed in U.S.A. A0357A-02U8905/SE EN

FLUKE